#6

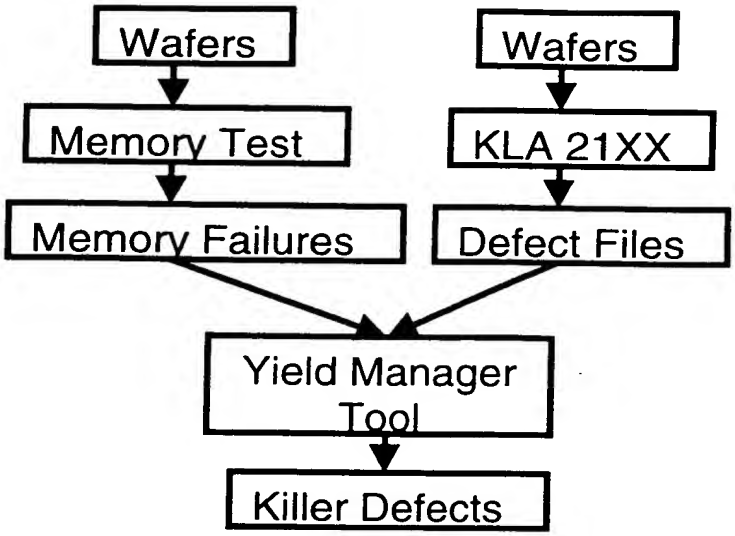


FIG 1
(PRIOR ART)

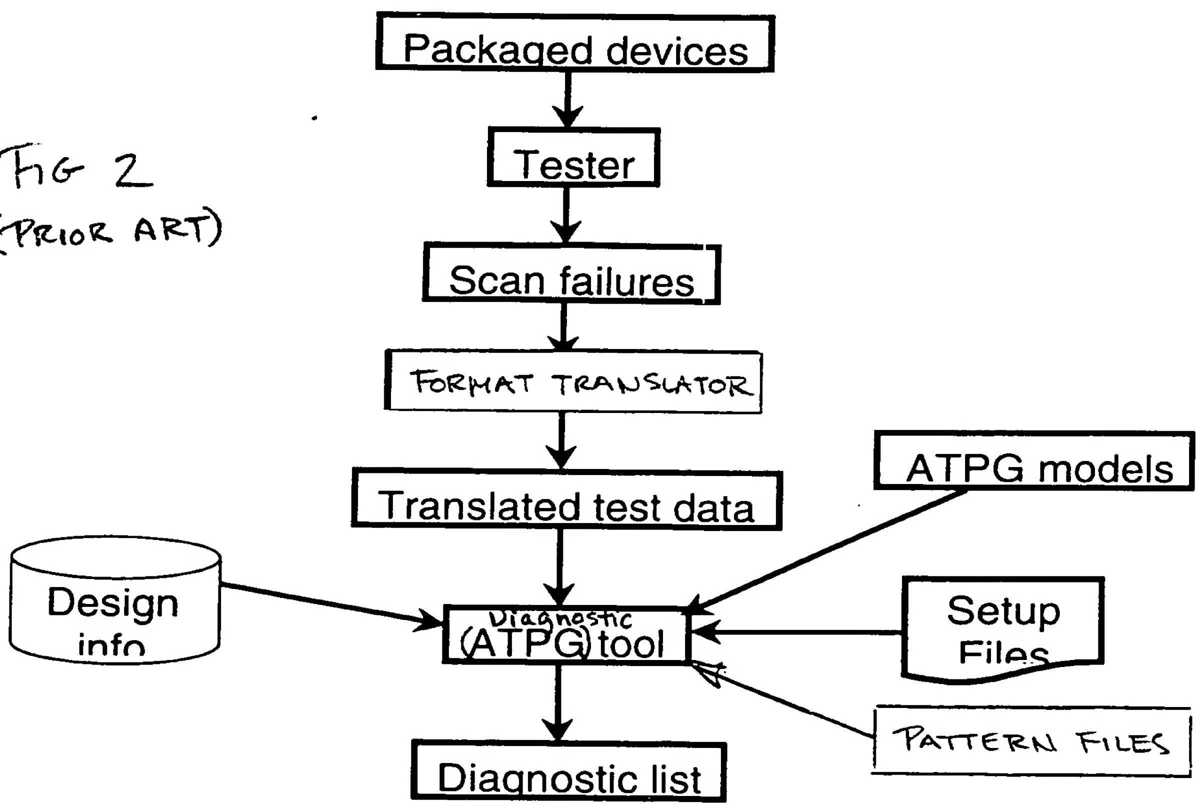


FIG 2
(PRIOR ART)

```
DeviceID = DEMOID
LotID = TESTLOT01
WaferID = 01
DIE = -4,0
datalog.scan.10 diagnosis summary, #failing_patterns=9  #defects=2
#unexplained_fails=2
unexplained patterns = 212 250
-------------------------------------------------------------------------
fault candidates for defect 1,  #failing_patterns_explained=5
-------------------------------------------------------------------------
Warning: Fault candidates will cause passing patterns to fail.
failing patterns explained = 322 706 738 770
type   code   pin_pathname
----   ----   ------------------------------------
  1    DS     /XTIO_0/XTTLI8_1612/N2_23
  1    DS     /PI9
-------------------------------------------------------------------------
diagnosis CPU time = .68 sec
```

FIG 3 (PRIOR ART)

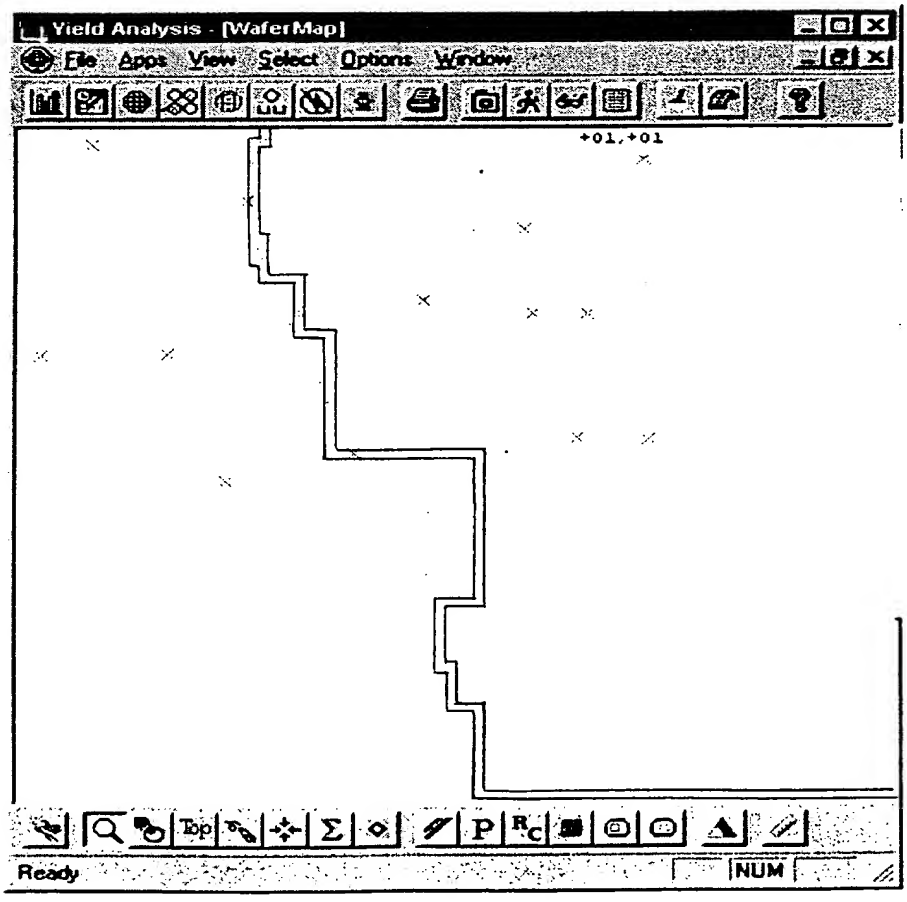


FIG 7

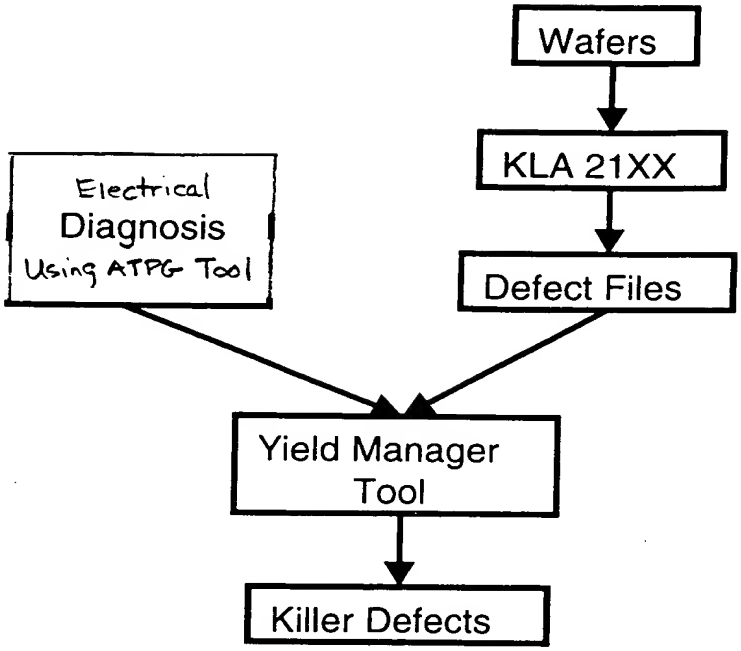

Wafers
KLA 21XX
Defect Files
Electrical
Diagnosis
Using ATPG Tool
Yield Manager
Tool
Killer Defects

Fig. 5

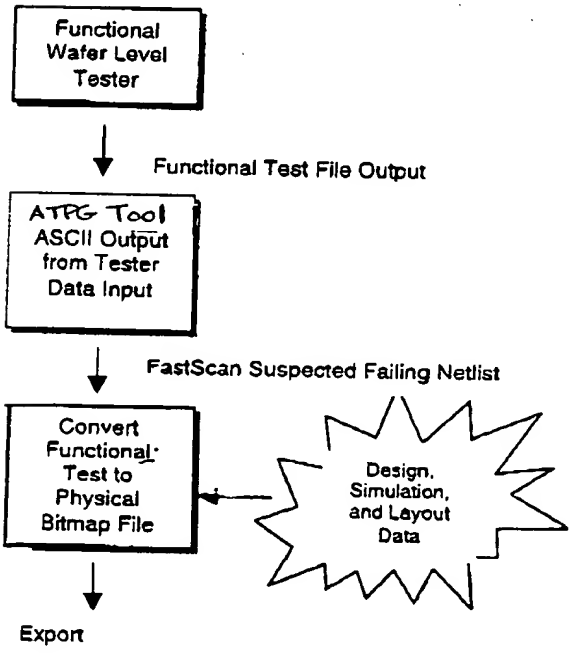
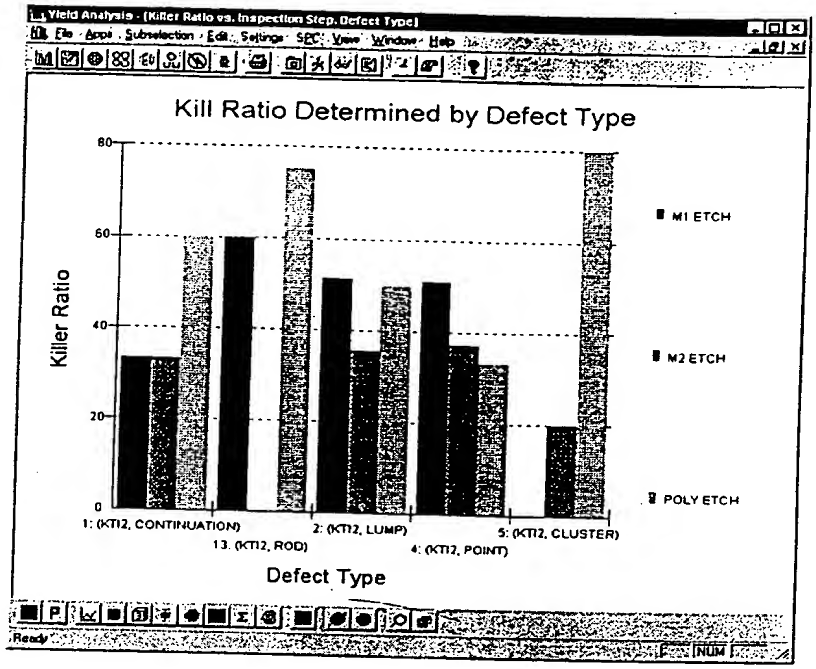

Functional
Wafer Level
Tester
Functional Test File Output
ATPG Tool
ASCII Output
from Tester
Data Input
FastScan Suspected Failing Netlist
Convert
Functional
Test to
Physical
Bitmap File
Design,
Simulation,
and Layout
Data
Export

Fig. 6

Fig 8


Yield Analysis - [Killer Ratio vs. Inspection Step. Defect Type]
File Appl Subselection Edit Settings SPC View Window Help
Kill Ratio Determined by Defect Type
Killer Ratio
80
60
40
20
0
M1 ETCH
M2 ETCH
POLY ETCH
1: (KTI2, CONTINUATION)
13: (KTI2, ROD)
2: (KTI2, LUMP)
4: (KTI2, POINT)
5: (KTI2, CLUSTER)
Defect Type
Ready
NUM

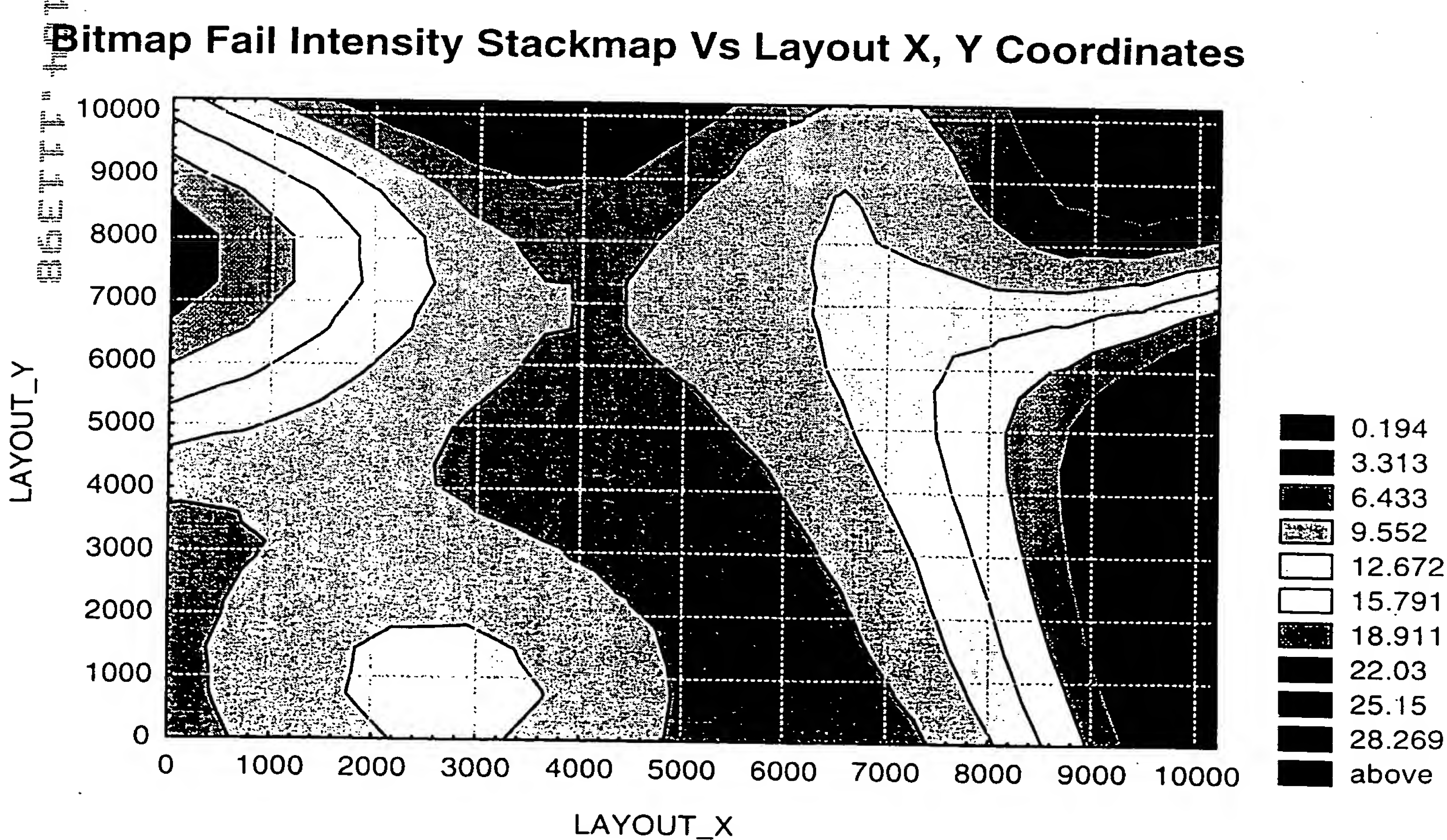

Bitmap Fail Intensity Stackmap Vs Layout X, Y Coordinates
LAYOUT_Y
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000
LAYOUT_X
0.194
3.313
6.433
9.552
12.672
15.791
18.911
22.03
25.15
28.269
above

Fig 9

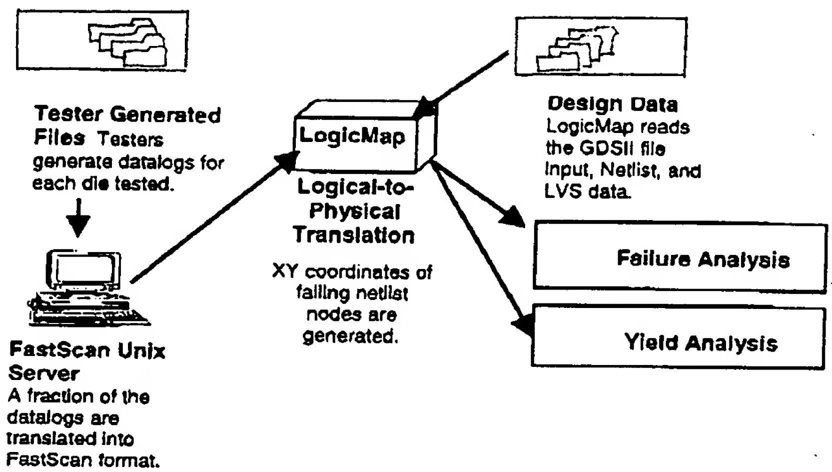

Tester Generated Files Testers generate datalogs for each die tested.
FastScan Unix Server
A fraction of the datalogs are translated into FastScan format.
LogicMap
Logical-to-Physical Translation
XY coordinates of failing netlist nodes are generated.
Design Data
LogicMap reads the GDSII file input, Netlist, and LVS data.
Failure Analysis
Yield Analysis

FIG 10

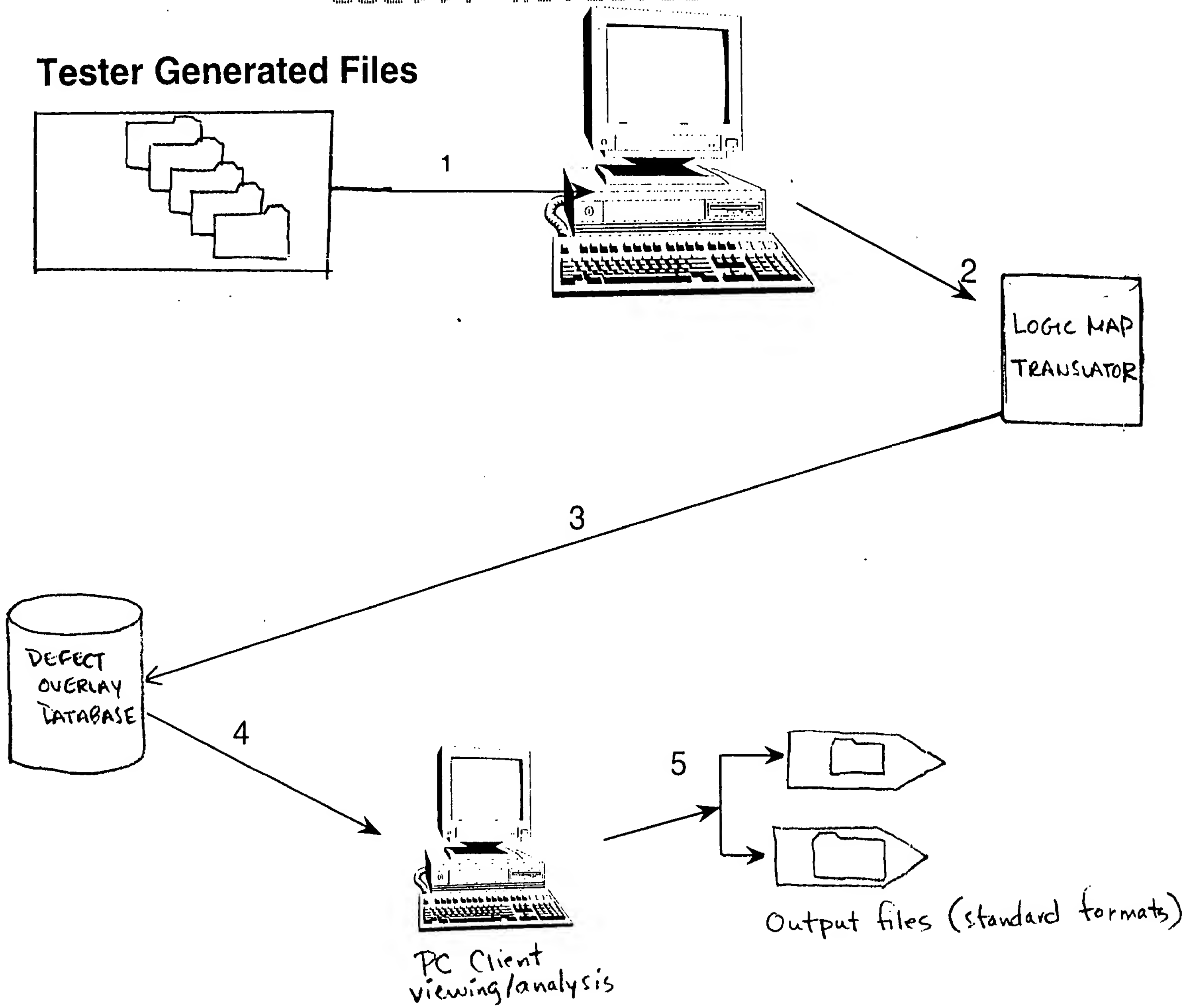


FIG 11

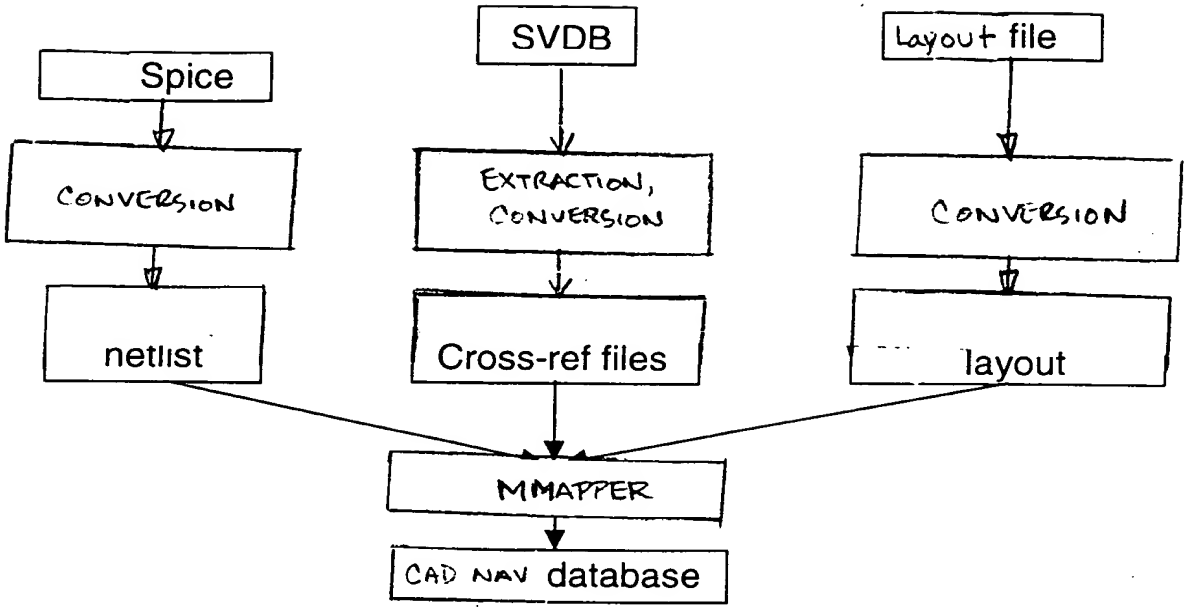


FIG 4 (PRIOR ART)

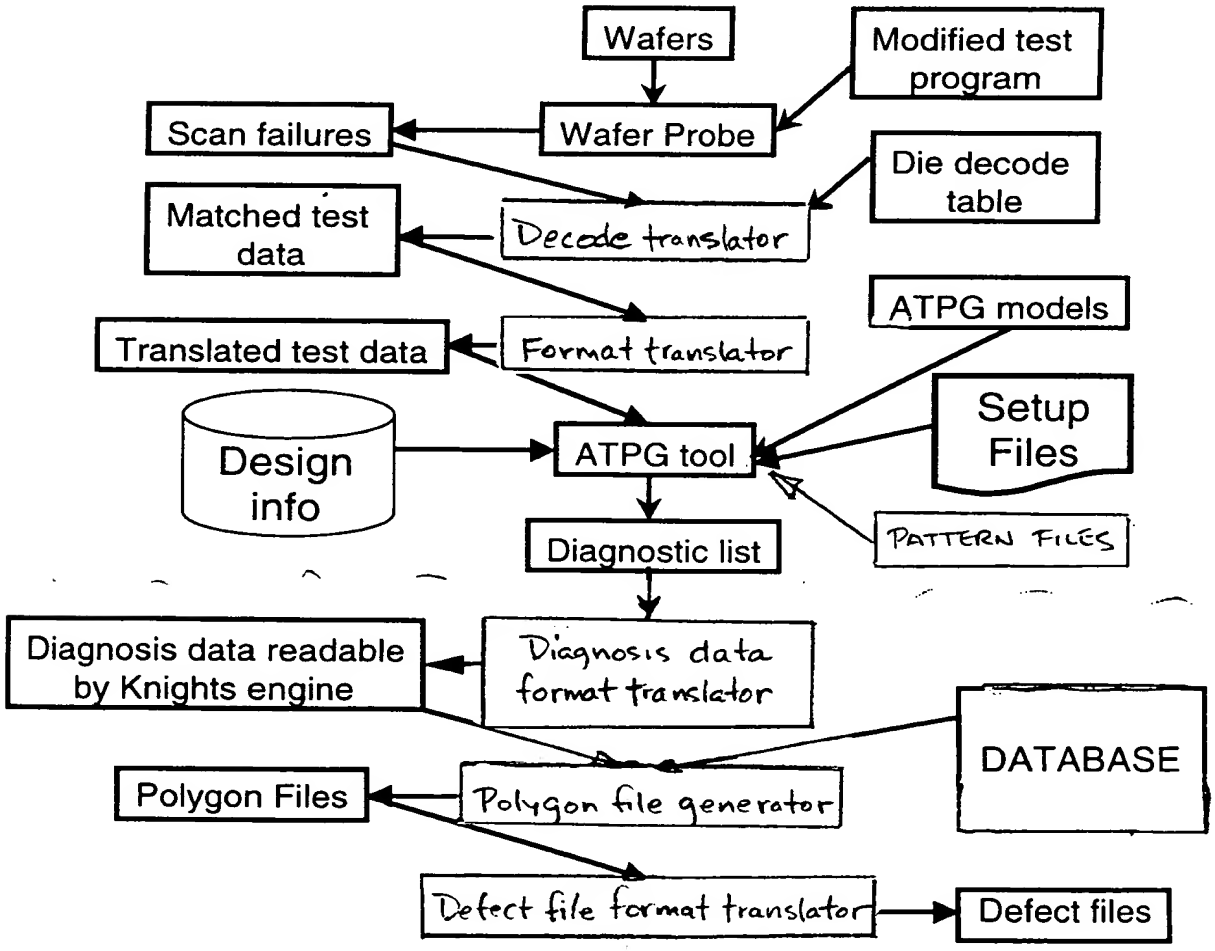


FIG 12